

Remarks

Reconsideration and allowance of this Application is respectfully requested.

In the amendment set forth above, Claims 1, 3, 5, 7-9, 15, and 16 are amended; and Claims 10-13, 20, 21, 24, 26, and 31-37 are Original; Claims 6, 14, 22, 25, 27, 28, and 30 were Previously Presented; and Claims 2, 4, 17-19, and 29 have been cancelled.

Amendments have been made in the Claims to more clearly define the various scopes and aspects of the invention. These amendments are supported by the Specification and Drawings and no new matter has been added. These amendments are made (i) for clarification purposes; (ii) not for purposes of delay; and (iii) not to overcome or define over any cited art; and, accordingly, these amended Claims should be afforded the full scope and range of interpretation.

In view of the amendments to the Claims and the Remarks and Arguments set forth below, it is respectfully submitted that all of the Claims are currently in condition for allowance, and a Notice of Allowance is respectfully requested.

1. The withdrawal of indicated allowability of Claim 4 on newly cited art is acknowledged.

2. The provisions of 35 USC 102(b) are duly noted.

3. The rejection of Claims 1, 3, 6 -16, 19 28, and 30 - 37 under 35 USC §102(b) as being anticipated by U.S. Pat. No. 5,644,753 to Ebrahim, et al. ("Ebrahim") is respectfully traversed.

Before addressing the specific rejections, it will be beneficial to consider Ebrahim with regard to what is taught and what is not taught. Ebrahim teaches a dual port cache controller, wherein a first port receives access requests from a system controller. The cache memory access requests include an address, access requests, and a mode flag. A comparator evaluates the address value and determines hit/miss depending upon the data block corresponding to the address is in the cache. The cache controller has two modes of operation, with a first mode in which read/write access is preceded by hit/miss determination, and

/2

a second mode in which read/write access to the cache proceeds without waiting for the hit/miss evaluation. The accelerated or second mode can be utilized when it is predetermined that addressed data will be written in the cache. Etag is the array of cache tags for a cache memory and are accessed and updated by a processor. Dtag is a duplicate of the Etag and is maintained by the system controller. The Etag cache states can include a number of cache transitions, for example see Column 27.

Ebrahim does not teach or suggest that a programmable storage device can be utilized for storage of indicators, nor that the indicators can be programmably altered. Further, Ebrahim does not appear to teach or suggest the use of a mode switch to re-program one of the indicators.

Turning to the Office Action, the finding with respect to Claim 1 that Ebrahim teaches a "programmable storage device" to store indicators, directs attention Etag and Dtag, Fig. 1 and Fig. 12 for storing line identifier, and to Col. 4, lines 1-5, Col. 13, Lines 37-66. The referenced drawings and descriptive material do describe the storage of cache tags (Etag) and the storage of duplicate cache tags (Dtag), but there is no teaching of a "programmable" storage device. There is no need for a "programmable" storage device because the function described above is designed into the structure. In contradistinction, Applicants describe and claim a system that has programmable characteristics. In this regard see Applicants' Drawings and for illustrative teachings, see page 5, lines 13-18; page 15, lines 9-14; page 17, lines 3-13; page 28, lines 3-12; page 34, lines 6-17; and the descriptive material regarding Figure 2. The foregoing is not intended to be exhaustive, but these references provide descriptions that differentiate the system herein claimed from that taught by Ebrahim.

In summary, Ebrahim is an example of the prior art systems described by Applicants as prior art, wherein the various features and functionalities are designed fixed in the system, as opposed to the system claimed by Applicants, wherein the functionality and responses may be programmably modified to meet various system requirements, requirements of different software solutions using

the system, reconfigurations of hardware, and the like, all with the benefit of enhancing performance in the various different situations.

Ebrahim does not teach all of the elements of Claim 1, and, accordingly it is allowable as presently presented.

Claims 3, 5, 6, 7, and 8 each depend from Claim 1, and claim different scopes and aspects of the invention, all of which benefit from the structure claimed in Claim 1. Accordingly, each is allowable for the reasons set forth above.

Dependent Claims 14 and 15 also depends from Claim 1, and have not been considered by the Examiner as part of the current rejection, other than on a perfunctory basis. It is submitted that Claim 14 further defines the programmable storage device to include circuits to store microcode, and Claim 15 further deals with programming of indicators, neither of which are taught or suggested by Ebrahim. For these reasons and the reasons provided above, Claims 14 and 15 are allowable. If the Examiner persists in rejection of these claims, it is respectfully requested that specific reasons for rejection be provided.

Independent Claim 9 has been amended herein, and is neither taught nor suggested by Ebrahim, and at least for the reasons set forth above, it is allowable as presently presented.

Claims 10-13 depend either directly or indirectly from Claim 9, and claim various aspects and combinations that are neither taught nor suggested by Ebrahim. These Claims are not co-extensive with Claim 1 and the Claims that depend from Claim 1. Should the Examiner persist in rejecting these Claims, it is respectfully submitted that they be specifically considered and definite rejections made. For the foregoing reasons, Claims 10-13 are allowable as presently presented.

Independent Claim 16 has been amended to include the limitation of Claim 19. The claimed method includes operating and controlling a memory system that has programmable control indicators, and includes method steps that are neither taught nor suggested by Ebrahim, and is therefore now in condition for allowance. Again Claim 16 is not coextensive with Claim 1, and should the

Serial No. 10/620,406
Unisys Corporation Docket No. RA-5623

Examiner Pierre Bataille, Group Art Unit 2186
Office Action Response - June 30, 2008

Examiner persist in a rejection, it is respectfully requested that reasons specific to Claim 19 be given to support any such rejection.

Claims 20-26 depend directly or indirectly from Claim 19 and are allowable for the reasons set forth above.

Independent Claim 27 has not been specifically examined with respect to Ebrahim. For the reasons set out herein and for the added reason that Ebrahim neither teaches nor suggest automatically re-programming and of the control indicators based on monitored conditions, Claim 27 is allowable. If the Examiner persists in rejecting Claim 27, it is requested that examination be specifically applied.

Independent Claim 28 is written in means plus function terms and has not been examined as such. It is submitted that Ebrahim does not teach or suggest the limitations of Claim 28 when examined in accordance with applicable law. Clearly, Claim 28 is not of the same scope nor is it relative to the same aspects of Claims 1. Accordingly, if the Examiner persists in rejecting Claim 28, it is requested that examination be specifically applied. It is submitted that for the reasons set forth herein Claim 28 is allowable.

Claims 30-37 all depend directly or indirectly from Claim 28, and are allowable for the reasons set forth herein.

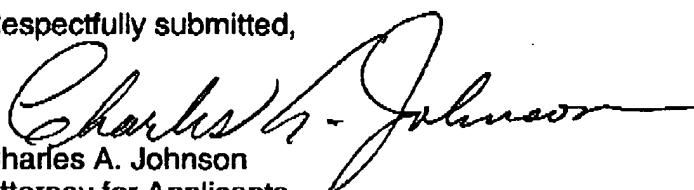
Serial No. 10/620,406
Unisys Corporation Docket No. RA-5623

Examiner Pierre Bataille, Group Art Unit 2188
Office Action Response - June 30, 2008

Conclusion

Claims 1, 3, 5, 7-9, 15, and 16 are amended; and Claims 10-13, 20, 21, 24, 26 and 31-37 are Original; Claims 6, 14, 22, 25, 27, 28, and 30 were Previously Presented; and Claims 2, 4, 17-19, and 29 have been cancelled. In view of the arguments presented, it is submitted that all Claims are in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner has any questions regarding the subject Application or this response, a call to the undersigned is encouraged and welcomed.

Respectfully submitted,


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16